Design of Multiply and Accumulate Unit using Vedic Multiplication Techniques

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Abstract— This paper proposed the design of Multiply and Accumulate (MAC) Unit using the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance. The speed of MAC depends greatly on the multiplier. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. The work has proved the efficiency of Urdhva Triyagbhyam– Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels using Karatsuba algorithm with the compatibility to different data types. Multiply-Accumulate is an extensible block using the Vedic multiplier module plays an important role in computing, especially digital signal processing. The coding is done in Verilog HDL and the FPGA synthesis is done using Xilinx Spartan library. The results show that design of MAC unit using Vedic multiplication is efficient in terms of area/speed compared to conventional multiplication.

Index Terms— FPGA Synthesis, Karatsuba - Ofman algorithm, Urdhva Triyakbhyam Sutra, Vedic Mathematics, Verilog HDL, Vedic Multiplier, Wallace Tree.

1 INTRODUCTION

THE Multipliers have an important effect in designing arithmetic, signal and image processors. Many mandatory functions in such processors make use of multipliers (for example, the basic building blocks in Fast Fourier transforms (FFTs) and multiply accumulate (MAC) are multipliers). The advanced digital processors now have fast bit-parallel multipliers embedded in them.

Various methods exist for the reduction in the computation time involved by the multiplier with other factors as trade-offs. High-speed, bit-parallel multiplication can be classified into three types (a) shift-and-add multipliers that generate partial products sequentially and accumulate. This requires more hardware and is the slowest multiplier. This is basically the array multiplier making use of the classical multiplying technique which consumes more time to perform two subtasks, addition and shifting of the bits and hence consumes 2 to 8 cycles of clock period. (b) generating all the partial product bits in parallel and accumulate them using a multi-operand adder. This is also called as parallel multiplier by using the techniques of Wallace tree [1] and Booth algorithm[2], (c) using arrays of almost identical cells for generation of bit products and accumulation.

The uses of Vedic Mathematics shows its application in fast calculations (multiplication, division, squaring, cubing, square root, cube root), trigonometry, three dimensional coordinate geometry, solution of plane and spherical triangles, linear and non-linear differential equations, matrices and determinants, log and exponential[15]. The most interesting point is to note that the Vedic Mathematics provides unique solutions in several instances where trial and error method is available at present.

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Vedic Mathematics offers a fresh and highly efficient approach to mathematics covering a wide range - starts with elementary multiplication and concludes with a relatively advanced topic, the solution of non-linear partial differential equations. But the Vedic scheme is not simply a collection of rapid methods; it is a system, a unified approach.

This paper proposes a multiplier providing the solution of the aforesaid problems adopting the sutra of Vedic Mathematics called Urdhva Tiryakbhyam (Vertically and Cross wise)[3,4,5]. It can be shown that the design MAC unit is highly efficient in terms silicon area/speed.

2 VEDIC MATHEMATICS

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful [2, 3].

The word "Vedic" is derived from the word **"Veda"**

which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically.

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2) Chalana-Kalanabyham – Differences and Similarities.
3) Ekadhikina Purvena – By one more than the previous One.
4) Ekanyunena Purvena – By one less than the previous one.
5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6) Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7) Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8) Paraavartya Yojayet – Transpose and adjust.
9) Puranapuranabyham – By the completion or noncompletion.
10) Sankalana- vyavakalanabhyam – By addition and by subtraction.
11) Shesanyankena Charamena – The remainders by the last digit.
12) Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14) Urdhva-tiryagbhyam – Vertically and crosswise.
15) Vyashtisamanstih – Part and Whole.
16) Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing [1,4].

The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial- parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

3 Design Of Proposed MAC Unit

3.1 Urdhva– Triyagbhyam (Vertically and Crosswise)

Urdhva tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional methods already know to us will require 16 multiplications and 15 additions.

An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown in Fig. 1. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

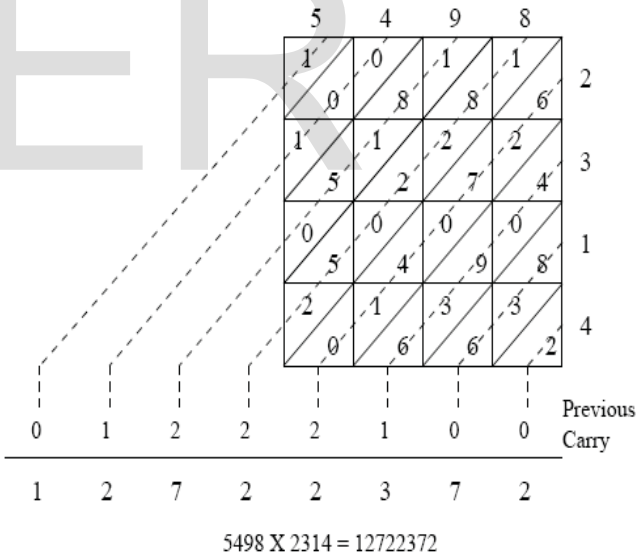


Fig.1 : Alternative way of multiplication by Urdhva tiryakbhyam Sutra.

The design starts first with Multiplier design, that is 2x2 bit multiplier as shown in figure 2. Here, "Urdhva Tiryakbhyam Sutra" or "Vertically and Crosswise Algorithm"[4] for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication, that is to add and shift the partial products.

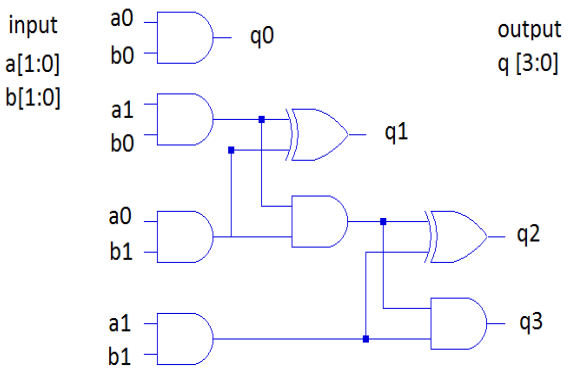


Fig.2 : Hardware Realization of 2x2 block

To scale the multiplier further, Karatsuba – Ofman algorithm can be employed[6]. Karatsuba-Ofman algorithm is considered as one of the fastest ways to multiply long integers. It is based on the divide and conquer strategy[11]. A multiplication of 2n digit integer is reduced to two n digit multiplications, one (n+1) digit multiplication, two n digit subtractions, two left shift operations, two n digit additions and two 2n digit additions.
The algorithm can be explained as follows:

Let X and Y are the binary representation of two long integers:

$$X = \sum_{i=0}^{k-1} x_i 2^i$$

$$Y = \sum_{i=0}^{k-1} y_i 2^i$$

We wish to compute the product XY. Using the divide and conquer strategy, the operands X and Y can be decomposed into equal size parts X*H* and X*L*, Y*H* and YL, where subscripts H and L represent high and low order bits of X and Y respectively.

Let k= 2n. If k is odd, it can be right padded with a zero

$$X = 2^n \sum_{i=0}^{n-1} x_{i+n} 2^i + \sum_{i=0}^{n-1} x_i 2^i = X_H 2^n + X_L$$

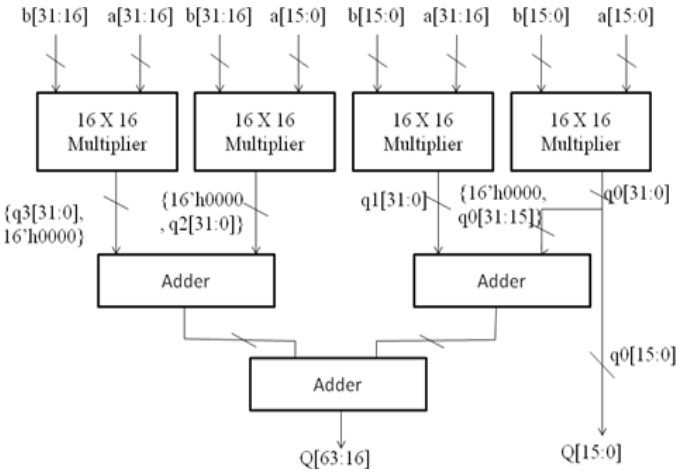
$$Y = 2^n \sum_{i=0}^{n-1} y_{i+n} 2^i + \sum_{i=0}^{n-1} y_i 2^i = Y_H 2^n + Y_L$$

The product XY can be computed as follows:

$$P = X * Y$$
$$= (X_H 2^n + X_L)(Y_H 2^n + Y_L)$$
$$= 2^{2n}(X_H * Y_H) + 2^n((X_H * Y_L) + (X_L * Y_H)) + (X_L * Y_L)$$

For Multiplier, first the basic blocks, that are the 2x2 bit multipliers have been made and then, using these blocks, 4x4 block has been made and then using this 4x4 block, 8x8 bit block, 16x16 bit block and then finally 32 x 32 bit Multiplier as shown in figure 3has been made[7].

Fig.3: Block diagram of 32x32 Multiply block



3.2 MAC

The MAC unit is built with Vedic multiplier. Hence the advantages of Vedic multiplier like increase in speed, decrease in delay, decrease in power consumption, decrease in area occupied will enhance the MAC unit also. The DSP applications like Convolution (summation of multiplied terms), Correlation, Discrete Fourier Transform, Fast Fourier Transform etc employ the MAC unit, which assists in efficient computing in terms of speed, delay and complexity.

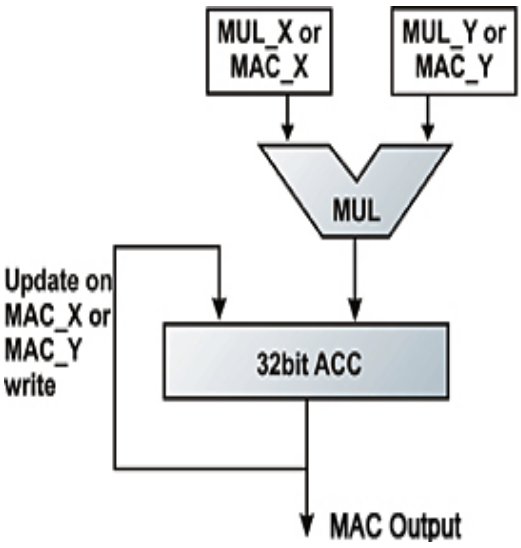


Fig.4 : Multiply and Accumulate Unit

4 Performanec Evaluvation And Comparison

The proposed MAC unit is implemented using two different coding techniques viz., Wallace tree and Vedic technique for 32 bit multiplier. It is evident that there is a considerable increase in speed of the Vedic architecture. The simulation results for 32 bit multiply and accumulate unit is shown in the figure 5

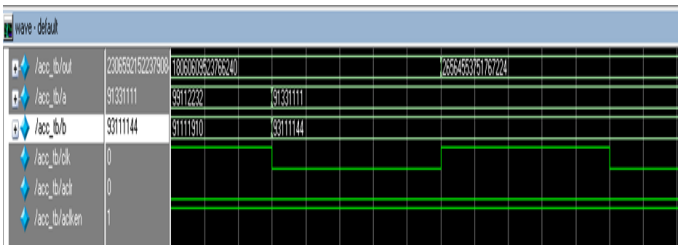


Fig 5: Simulation result of MAC Unit

TABLE 1

DELAY COMPARISION FOR DIFFERENT MAC UNITS

Performance	MAC unit using Wallace Tree	MAC unit using Vedic Multiplier
Minimum Period (ns)	64.624ns	37.799ns
Area (No. of LUTs)	3172	2714

The worst case propagation delay in the Optimized MAC unit using Vedic multiplier case was found to be 37.799ns. To compare it with other implementations the design was synthesized on XILINX: SPARTAN: xc3s500e-5fg320[18]. Table 1 shows the synthesis result for various implementations. The result obtained from proposed MAC unit using Vedic multiplier is faster than MAC unit using Wallace Tree.

5 Conclusion

In this paper, a new method of 32-bit MAC unit is presented based on Vedic method of multiplication [9]. This gives us method for hierarchical multiplier design. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased.. The Multiply and Accumulate Unit designed with Vedic overlay high speed multiplier algorithm exhibits improved efficiency in terms of speed and area.

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